AMENDMENTS TO THE CLAIMS

Please amend the claims as set forth in the following listing. This listing of claims will replace all prior versions, and listings, of claims for the present application:

Claims 1-54 (Canceled).

55.(Previously Presented) A process for using a photo-definable layer in a negative mask scheme to manufacture a semiconductor device, comprising:

forming over a substrate a photo-definable layer that is convertible to an insulative material;

exposing selected portions of said photo-definable layer to electro-magnetic radiation in a negative pattern scheme to convert said selected portions to an insulative material;

removing non-exposed portions of said photo-definable layer with an etch process that is selective to exposed portions of said photo-definable layer;

using said exposed portions of said photo-definable layer as a patterned etch mask for further processing steps;

leaving said exposed portions of said photo-definable layer as an insulative layer within said semiconductor device after completion of the use of said exposed portions of said photo-definable layer as a patterned etch mask; and

converting said insulative layer to an oxide layer through exposure to an oxygen plasma after said leaving step.

56.(Previously Presented) The process of claim 55, wherein said photo-definable layer comprises an organosilicon resist.

57. (Previously Presented) The process of claim 56, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

Claims 58-75 (Canceled).

76. (Currently Amended) A process of using a photo-definable layer in a Damascene process to create a patterned structure, comprising:

forming on a substrate a photo-definable layer that is convertible to an insulative material;

exposing selected portions of said photo-definable layer to electro-magnetic radiation to convert said selected portions to an insulative material;

removing non-exposed portions of said photo-definable layer with an etch process that is selective to exposed portions of said photo-definable layer to form a desired pattern within said exposed portions of said photo-definable layer;

leaving said exposed portions of said photo-definable layer on said substrate as an insulative layer ~~after completion of the etch process~~ after completion of the use of said exposed portions of said photo-definable layer as a patterned etch mask; and

converting said insulative layer to an oxide layer through exposure to an oxygen plasma after said leaving step.

77. (Previously Presented) The process of claim 76, wherein said photo-definable layer comprises an organosilicon resist.

78. (Previously Presented) The process of claim 77, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

79. (Previously Presented The process of claim 78, further comprising consolidating said oxide layer with an anneal.

80. (Previously Presented) The process of claim 79, further comprising depositing a conductive material within said pattern.

81. (Previously Presented) The process of claim 80, wherein said conductive material forms an interconnect structure within a semiconductor memory device.

82. (Previously Presented) The process of claim 76, wherein said exposing step is performed by irradiating said selected portions of said photo-definable layer with ultraviolet light in the presence oxygen.

83. (Previously Presented) The process of claim 82, wherein said non-exposed portions of said photo-definable layer are removed using a chlorine-based or a bromine-based plasma etch.

Claims 84-100 (Canceled).

101. (New) The process of claim 56, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

102. (New) The process of claim 76, further comprising forming a conductive layer inlaid within the oxide layer.

103. (New) The process of claim 102, wherein said conductive layer forms an interconnect structure within a semiconductor memory device.